IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

FLASH-CONTROL, LLC,	§	
Plaintiff,	§	
	§	**CIVIL ACTION 1:19-cv-01107-ADA**
v.	§	
	§	**JURY TRIAL DEMANDED**
INTEL CORPORATION,	§	
Defendant.	§	

CLAIM CONSTRUCTION ORDER AND ORDER
GRANTING DEFENDANT INTEL'S MOTION FOR SUMMARY JUDGMENT

Came on for consideration this date the Motion of Defendant Intel Corporation ("Intel") for Summary Judgment under FED. R. CIV. P. 56(a) and opening claim construction brief filed on February 5, 2020. ECF No. 48. Plaintiff Flash-Control, LLC ("Flash-Control") responded on April 23, 2020 (ECF No. 60) and Intel replied on May 5, 2020 (ECF No. 63). The Court held a combined Summary Judgment and Markman hearing on June 5, 2020. During that hearing, the Court orally granted Intel's Motion for Summary Judgment and provided the Parties with its final construction for one term. This Order does not alter that construction. For the reasons that follow, the Court **GRANTS** Intel's motion for summary judgment.

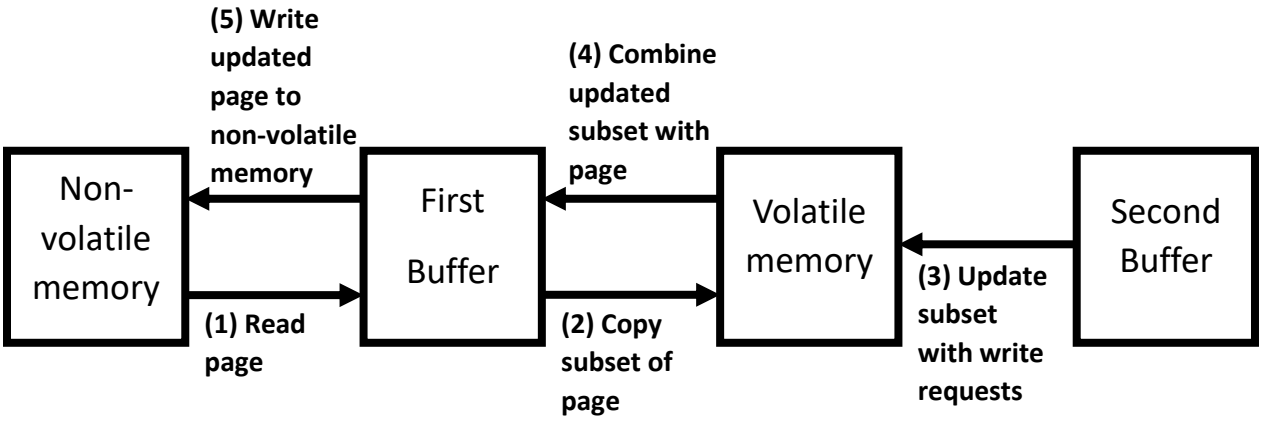
I. BACKGROUND

Flash-Control filed this lawsuit alleging that Intel infringed U.S. Patent Nos. 8,531,880 (the '880 Patent) and 8,817,537 (the '537 Patent). ECF No. 1 at ¶ 16. Both patents are titled "Nonvolatile Memory Systems with Embedded Fast Read and Write Memories." ECF No. 1 at ¶¶ 8, 11. The '537 Patent is a continuation of the '880 Patent, and they share a common specification. ECF No. 48 at 9. The patents are generally directed to the coupling of nonvolatile memory with random access volatile memory to enhance the read and write performance of a memory system.

ECF No. 1 at ¶ 19, 31. These patents purportedly provide an improved structure and computing environment for memory systems. ECF No. 1 at ¶ 20.

The claimed inventions in the '880 and '537 Patents aggregate and combine write requests in order to reduce the number of writes to nonvolatile memory, which improves the read time and write time while also increasing the lifetime of the nonvolatile memory. '880 Patent at 1:63–66. More specifically, the '880 and '537 Patents claim a memory system that includes nonvolatile memory (*e.g.*, flash memory), a first buffer to store a memory page, volatile memory (*e.g.*, SDRAM), and a second buffer. *See, e.g.*, '880 Patent at Cl. 1.

Claim 1 of the '880 Patent generally recites five steps. ***First***, the nonvolatile memory reads the page associated with a write request and writes that page to the first buffer. *Id.* at Cl. 1, Lim. [e]. ***Second***, the first buffer copies a subset of the page to the volatile memory. *Id.* at Cl. 1, Lim. [f]. ***Third***, the second buffer, which stores information associated with write requests, updates the subset of the page in volatile memory with the write requests for that subset. *Id.* at Cl. 1, Lims. [d, g]. ***Fourth***, the volatile memory writes the updated subset into the page in the first buffer. *Id.* at Cl. 1, Lim. [g]. ***Fifth***, the first buffer writes the updated page back into the nonvolatile memory. *Id.* at Cl. 1, Lim. [h]. The following diagram depicts these five steps and the interrelationship between the nonvolatile memory, the first buffer, the volatile memory, and the second buffer.



Intel filed a Motion for Summary Judgment pursuant to FED. R. CIV. P. 56(a) alongside its opening construction brief. ECF No. 48. Intel requests judgment in its favor on the grounds that the '880 and '537 Patents are invalid for a lack of a written description. *Id.* at 21. Intel also argues that Claim 1 of the '880 Patent is indefinite. *Id.*

II. LEGAL STANDARD

a. Summary Judgment

Summary judgment is appropriate "if the movant shows that there is no genuine dispute as to any material fact and the movant is entitled to judgment as a matter of law." FED. R. CIV. P. 56(a); *Tolan v. Cotton*, 572 U.S. 650, 656–57 (2014). A material fact will have a reasonable likelihood to affect the outcome of the case. *Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 248 (1986). An issue is not genuine if the trier of fact could not, after an examination of the record, rationally find for the non-moving party. *Matsushita Elec. Indus., Co. v. Zenith Radio Corp.*, 475 U.S. 574, 587 (1986). As such, the burden of demonstrating a lack of a genuine dispute of material fact lies with the movant. *Celotex Corp. v. Catrett*, 477 U.S. 317, 323 (1986).

Once presented, a court must view the movant's evidence and all factual inferences from such evidence in a light most favorable to the party opposing summary judgment. *Impossible Elecs. Techniques v. Wackenhut Protective Sys., Inc.*, 669 F.2d 1026, 1031 (5th Cir. 1982). Accordingly, the fact that the court believes that the non-moving party will be unsuccessful at trial is an insufficient reason to grant summary judgment in favor of the moving party. *Jones v. Geophysical Co.*, 669 F.2d 280, 283 (5th Cir. 1982). However, "[w]hen opposing parties tell two different stories, but one of which is blatantly contradicted by the record, so that no reasonable jury could believe it, a court should not adopt that version of the facts for the purposes of ruling on a motion for summary judgment." *Scott v. Harris*, 550 U.S. 372, 380–81 (2007).

Once the court determines that the movant has presented sufficient evidence that no genuine dispute of material fact exists, the burden of production shifts to the party opposing summary judgment. *Matsushita*, 475 U.S. at 586. The non-moving party must demonstrate a genuinely disputed fact by citing to parts of materials in the record, such as affidavits, declarations, stipulations, admissions, interrogatory answers, or other materials; or by showing that the materials cited by the movant do not establish the absence of a genuine dispute. FED. R. CIV. P. 56(c)(1)(A)–(B). "Conclusory allegations unsupported by concrete and particular facts will not prevent an award of summary judgment." *Duffy v. Leading Edge Prods.*, 44 F.3d 308, 312 (5th Cir. 1995).

b. Written Description

Under Section 112, Paragraph 1 of the Patent Act, "[t]he specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same." 35 U.S.C. § 112, ¶ 1. "The test for the sufficiency of the written description 'is whether the disclosure of the application relied upon reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date.'" *Vasudevan Software v. MicroStrategy, Inc.*, 782 F.3d 671, 682 (Fed. Cir. 2015) (quoting *Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (*en banc*)). "[T]he test requires an objective inquiry into the four corners of the specification from the perspective of a person of ordinary skill in the art." *Vasudevan*, 782 F.3d at 682 (citing *Ariad*, 598 F.3d at 1351). Whether the written description adequately supports a patent claim is a question of fact. *Id.* (citing *Ariad*, 598 F.3d at 1355). "A party must prove invalidity for lack of written description by clear and convincing evidence." *Id.*

c. Claim Construction

The general rule is that claim terms are generally given their plain-and-ordinary meaning. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*); *Azure Networks, LLC v. CSR PLC*, 771 F.3d 1336, 1347 (Fed. Cir. 2014), *vacated on other grounds*, 575 U.S. 959, 959 (2015) ("There is a heavy presumption that claim terms carry their accustomed meaning in the relevant community at the relevant time."). The plain and ordinary meaning of a term is the "meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Philips*, 415 F.3d at 1313.

"Although the specification may aid the court in interpreting the meaning of disputed claim language, particular embodiments and examples appearing in the specification will not generally be read into the claims." *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1571 (Fed. Cir. 1988). "[I]t is improper to read limitations from a preferred embodiment described in the specification—even if it is the only embodiment—into the claims absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited." *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004).

Although extrinsic evidence can be useful, it is "'less significant than the intrinsic record in determining the legally operative meaning of claim language.'" *Phillips*, 415 F.3d at 1317 (quoting *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 862 (Fed. Cir. 2004)). Technical dictionaries may be helpful, but they may also provide definitions that are too broad or not indicative of how the term is used in the patent. *Id.* at 1318. Expert testimony also may be helpful, but an expert's conclusory or unsupported assertions as to the meaning of a term are not. *Id.*

The "only two exceptions to [the] general rule" that claim terms are construed according to their plain and ordinary meaning are when the patentee (1) acts as his/her own lexicographer or

(2) disavows the full scope of the claim term either in the specification or during prosecution. *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012). To act as his/her own lexicographer, the patentee must "clearly set forth a definition of the disputed claim term," and "clearly express an intent to define the term." *Id.* To disavow the full scope of a claim term, the patentee's statements in the specification or prosecution history must represent "a clear disavowal of claim scope." *Id.* at 1366. Accordingly, when "an applicant's statements are amenable to multiple reasonable interpretations, they cannot be deemed clear and unmistakable." *3M Innovative Props. Co. v. Tredegar Corp.*, 725 F.3d 1315, 1326 (Fed. Cir. 2013).

d. Indefiniteness

"[I]ndefiniteness is a question of law and in effect part of claim construction." *ePlus, Inc. v. Lawson Software, Inc.*, 700 F.3d 509, 517 (Fed. Cir. 2012). Patent claims must particularly point out and distinctly claim the subject matter regarded as the invention. 35 U.S.C. § 112, ¶ 2. A claim, when viewed in light of the intrinsic evidence, must "inform those skilled in the art about the scope of the invention with reasonable certainty." *Nautilus Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 910 (2014). If not, the claim fails § 112, ¶ 2 and is invalid as indefinite. *Id.* at 901. Whether a claim is indefinite is determined from the perspective of one of ordinary skill in the art as of the time the application was filed. *Id.* at 911.

III. ANALYSIS

a. Invalidity for Lack of Written Description

Intel argues that the specification of the patents lacks a corresponding disclosure for multiple claimed limitations. ECF No. 48 at 2. Intel claims that the specification was drafted to describe the utilization of non-volatile memory as additional static random-access memory (SRAM) so that pages can be moved quickly between blocks. *Id.* Intel further contends that the

claims were later drafted to encompass something different, namely, modifying a portion of a page on volatile memory. *Id.* Intel asserts that the specification does not provide legally sufficient written description for this method in any of the claims in either patent. *Id.*

Intel points to three specific limitations relating to partial page modification that lack adequate written description. *Id.* at 14. First, Intel argues that the specification does not provide support for the claim regarding "a second buffer configured to receive information associated with one or more write requests, said write requests being associated with one or more changes to one or more portions of a page in said non-volatile memory, said one or more portions being less than the entirety of said page." *Id.* (citing '880 Patent at 5:1–6). Intel points out that some figures show one buffer paired with non-volatile memory, but no figure or description shows a second buffer that can store a write request. *Id.* Intel claims that the embodiment relates only to the claim scope of the earlier, non-asserted patents which has nothing to do with a second buffer or the writing of a portion of a page to non-volatile memory. *Id.* at 14–15.

Second, Intel also argues that the specification does not provide support for the claim "locate in said first buffer said one or more portions of said page associated with said one or more write requests, and to selectively write said one or more portions to said volatile memory without writing the entirety of said page in said first buffer to said volatile memory." *Id.* at 15 (citing '880 Patent at 5:11–16). This claim corresponds to the second step in the above diagram of Claim 1. Intel contends that the specification only describes the coupling of a buffer with a block of memory such that entire pages can be moved. *Id.* Intel asserts that a POSITA would not understand this disclosure to describe the writing of a portion of a page to volatile memory. *Id.* Intel states that the specification's reference to "new commands" that include "read byte out of page" and "write byte out of page" come the closest to a sufficient description. *Id.* (citing '880 Patent at 4:30–36; '537

Patent at 4:31–39). However, Intel argues that solely naming a command without an illustration of how the command functions does not provide sufficient description to a POSITA to understand that the inventor was in possession of that command. *Id.* at 16. Additionally, Intel contends that no further description exists regarding the selective writing of a portion of a page from the first buffer to the volatile memory. *Id.*

Third, Intel also argues that the specification fails to provide support for the claim limitation "to write said one or more changes from said second buffer to said volatile memory, thereby updating said one or more updated portions from said volatile memory to said first buffer, thereby updating said page stored therein to include said one or more changes associated with said one or more write requests." *Id.* (citing '880 Patent at 5:18–24). This claim corresponds to the third and fourth steps in the above diagram of Claim 1. As mentioned above, Intel argues that the patent does not provide a description that a POSITA could rely on to demonstrate that the patentee had possession of a second buffer or moving a portion of a page. *Id.* In addition, Intel reiterates that the specification's naming of "new commands" does not demonstrate to a POSITA that the inventor was in possession of this portion of the alleged invention. *Id.*

Flash-Control argues that the specification provides support for the claim limitations in question in both patents. ECF No. 60 at 2. In support of the first limitation in question, Flash-Control points to the presence of two buffers where the page buffer in Figure 9 of both patents acts as the first buffer and the read/write buffer acts as the second buffer. *Id*. at 5. Flash-Control also states that the second buffer does not need to store the write request as the claim only refers to the second buffer receiving information associated with one or more write requests. *Id.* at 6. Flash-Control also points to Figure 6 as evidence of two buffers as Figure 6 shows a data register and a cache register which can be synonymous with buffers. *Id.* Flash-Control alleges that a POSITA

would have understood that a data register can receive and store write requests. *Id.* at 7. Flash-Control also argues that the configuration features of the second buffer are supported through its reference to address decoding to the select memory locations in one or more memory or peripheral devices. *Id.* Flash-Control argues that a POSITA would have understood that address decoding allows for the reading and writing of portions of pages stored in memory such as a bit or byte. *Id.* Flash-Control also contends that address decoding can be understood to involve the storage of information associated with write requests such as the location of the data subject to the write request command. *Id.*

Flash-Control also argues that address decoding lends support to the second limitation in question. *Id.* at 8. As mentioned above, Flash-Control states that the specification's mention of address decoding circuitry allows for "locat[ing] in [a] first buffer . . . one or more portion of [a] page." *Id.* (citing '880 Patent at 2:1–3). Additionally, each block can have a tag address bit which allows the locating of a bit, i.e., a portion of a page. *Id.* Flash-Control also cites the "switch" disclosed in the shared specification as allowing for writing to volatile memory. *Id.* Flash-Control points to the disclosure that a page "can be read and written (random page access, random access within a page, serial access from a page etc.)" as additional support for writing a portion of a page. *Id.* (citing '880 Patent at 3:43–48). Flash-Control also contends that coupling a buffer to a block of memory and enabling entire pages to be moved does not prevent portions of a page from being moved as both meanings are included within the understanding of coupling for a POSITA. *Id.* at 8–9.

Flash-Control further argues that the third claim limitation draws similar support from the disclosures referenced above. *Id.* at 9. Since the third limitation covers substantially similar material as the first two claim limitations, Flash-Control reiterates its arguments regarding the

buffers in Figure 9, the disclosure of a switch that may access volatile and nonvolatile memory to move a portion of a page, the ability to read and write random access within a page and serial access for a page. *Id.* at 9–10. Flash-Control also repeats its arguments pertaining to the data register in Figure 3 acting as a second buffer capable of controlling read/write combinations, the description of the bit-by-bit or byte-by-byte reading and writing, and the coupling of buffers to a block of memory allowing for moving portions of a page. *Id.* at 10. Additionally, Flash-Control argues that the "new commands" referenced by Intel do not fall short of a written description as a POSITA would know that the commands refer to reading and writing portions of a page. *Id.* at 11.

In its reply, Intel argues that Flash-Control's response does not rebut Intel's showing that the asserted claims lack written description support. ECF No. 63 at 1. Intel also argues that Flash-Control's expert's opinion must be rejected as a matter of law because of the expert's improper use of the asserted claims to provide their own written description support. *Id.* at 3. Intel points out the admission of Flash-Control's expert of his application of the incorrect legal standard by relying on the content of the asserted claims in his written description analysis. *Id.* Intel points to Dr. Bagherzadeh's inability to say that the specification, along with what he identified as the relevant figures, provided a sufficient written description when considered without the text of the claims. *Id.* at 3–4 (citing Deposition of Dr. Nader Bagherzadeh ("Bagherzadeh Dep."), 240:21–241:13). Intel also relies on Dr. Bagherzadeh's concession that he used the figures in the patent, the text of the specification, and the claims as a "three-legged stool" and that he has not offered an opinion on the written description without these three legs. *Id.* at 4–5 (citing Bagherzadeh Dep., 218:20–219:15). Since the asserted patents are all continuations that claim priority to an earlier specification, Intel argues the patents' claims are not present in the original written description and cannot be relied upon for written description support as a matter of law. *Id.* at 3 (citing *Centocor*

Ortho Biotech, Inc. v. Abbott Labs., 636 F.3d 1341, 1350 (Fed. Cir. 2011); *Anascape, Ltd. v. Nintendo of America, Inc.*, 601 F.3d 1333, 1337 (Fed. Cir. 2010); *TurboCare Div. of Demag Delaval Turbomachinery Corp. v. Gen. Elec. Co.*, 264 F.3d 1111, 1118 (Fed. Cir. 2001)).

Intel also argues that Flash-Control's expert's opinion must also be rejected as a matter of law because the expert improperly sought to derive written description support from selected disclosures from the patent rather than identifying support for the claimed invention as an integrated whole. *Id.* at 7. Intel contends that Dr. Bagherzadeh analyzed the specification for obviousness rather than a written description by using individual components of the claims from different embodiments and examples to argue that a POSITA could put together the invention. *Id.* at 8 (citing Bagherzadeh Dep., 146:5–12; *Ariad*, 598 F.3d at 1352). Intel argues that Dr. Bagherzadeh could not testify that he looked for support for the integrated claims when questioned whether a POSITA would have understood the disparate figures and text to teach the claims as an integrated whole. *Id.* at 8–9 (citing Bagherzadeh Dep., 173:24–174:21).

Intel further argues that even if the Court credited Flash-Control's expert's opinion, Flash-Control's position fails on the merits for not meaningfully rebutting Intel's showing that the asserted claims lack written description support. *Id.* at 10. Intel's reply focuses on the third limitation presented in Intel's motion since the analysis of the third claim limitation encompasses the written description defects found in the first two limitations. *Id.* The third limitation has two key requirements: "(1) a second buffer that is configured to store information associated with a write request that modifies a portion of a page, and (2) a volatile memory that holds at least one partial page originating from the non-volatile memory, that can update that partial page based on information from the second buffer, and that can then write that updated information to the first buffer." *Id.* at 11.

Intel argues that Flash-Control has not identified any disclosure within the specification of these two elements individually or as an integrated whole with the rest of the claim. *Id.* Intel points to Flash-Control's claims that figures depicting two buffers and its supporting text discloses reading and writing a portion of a page. *Id.* However, Intel notes that relying on a collection of embodiments and examples selected from various parts of the specification as opposed to taking the specification as an integrated whole is not sufficient. *Id.* For example, Intel points to Dr. Bagherzadeh's testimony that the read/write buffer in Figure 9 does not disclose modifying portions of a page. *Id.* (citing Bagherzadeh Dep., 201:4–202:8). Moreover, even if Figure 9 did disclose modifying portions of a page, Intel asserts that the figure could not demonstrate that the inventor possessed a volatile memory that can "(1) hold at least one partial page originating from the non-volatile memory, (2) update that partial page based on information from the second buffer, and (3) write that updated information to the first buffer." *Id.* at 11–12. Intel points to Dr. Bagherzadeh's concession that Figure 9 does not show a first buffer, a second buffer, or a volatile memory as required by the claims. *Id.* at 12 (citing Bagherzadeh Dep., 194:20–24, 195:21–196:2). Intel further argues that Dr. Bagherzadeh admitted that the only way that he would conclude that the "read/write buffer" could be the second buffer was by improperly bootstrapping the disclosure with the claims themselves. *Id.* (citing Bagherzadeh Dep., at 202:23–205:13).

Intel points out that Flash-Control cites the data register in Figure 3 as "capable of controlling read/write combinations, thus, allowing movement and/or modification of pages or portions thereof" to support the requirement that the second buffer be able to store information associated with a write request that modifies a portion of a page. *Id.* (quoting ECF No. 60 at 10). However, Intel points to Dr. Bagherzadeh's admission that Figure 3 could only disclose a second buffer by combining the data register in Figure 3 with Figure 9. *Id.* (citing Bagherzadeh Dep.,

232:7–233:3, 236:10–237:7). Intel recognizes that Dr. Bagherzadeh could not testify that a POSITA would understand that Figure 3 and Figure 9 as an integrated whole would disclose the complete invention. *Id.* at 12–13.

Intel also contends that Flash-Control's conclusion that "the shared specification says that these portions of a page may be read or written, and writing is making a change" does not cite to the expert's declaration or testimony. *Id.* at 13 (quoting ECF No. 60 at 11). Intel argues that this unsupported argument does not address how a POSITA would understand "[r]andom access within a page and serial access from a portion of a page are examples of a portion of a page" to reflect possession of the claimed invention as an integrated whole. *Id* (quoting ECF No. 60 at 10).

Intel also points to Flash-Control's reliance on the commands "read byte out of page" and "write byte out of page" to "refer to reading and writing portions of a page." *Id.* (quoting ECF No. 60 at 11–12). Intel argues that "Flash-Control neither shows how these commands are linked to the first buffer, the second buffer, or the volatile memory nor how it shows possession by the named inventor of the claim limitations that describe the interaction of all three components." *Id.* Intel points out that Dr. Bagherzadeh could only conclude that the applicant was "in possession of a system in which portions smaller than an entire page could be selectively located and read or written." *Id.* (quoting ECF No. 60, Ex. 3, ¶ 46). Intel argues that Dr. Bagherzadeh does not conclude that the commands demonstrate that the applicant was in possession of the claimed system because the specification provides no explanation for their function. *Id.* at 13–14 (citing '880 Patent at 4:32–35).

Intel also recognizes Flash-Control's assertion of "a switch that may access volatile and nonvolatile memory to move a portion of a page" providing support for the written description. *Id.* at 14 (citing ECF No. 60 at 10 (quoting '880 Patent at 3:31–34)). However, Intel notes that Dr.

Bagherzadeh admits that the process of SRAM switching is not claimed and does not explain how a switch could "demonstrate possession of a second buffer, a volatile memory, and the claimed data flow between them." *Id.* (citing Bagherzadeh Dep., 285:15–17).

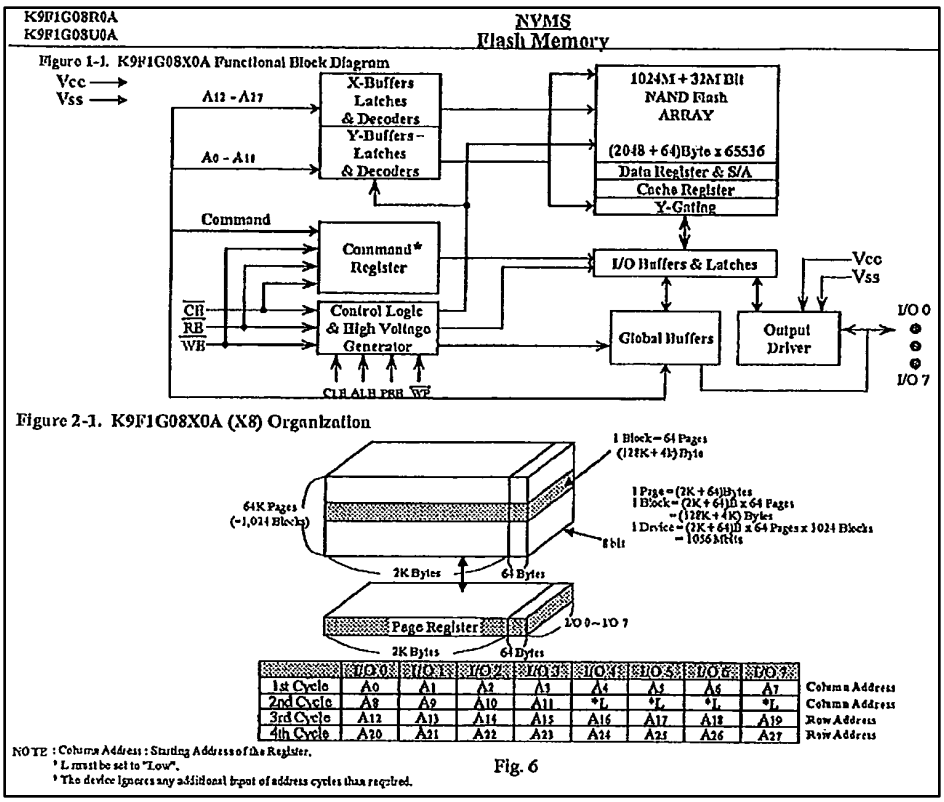
Intel further alleges that Flash-Control's identification of "coupling buffers" likewise falls short. *Id.* Intel points out that Flash-Control merely contends that coupling buffers may be used to move a page or a portion of a page. *Id.* (citing ECF No. 60 at 11). However, Intel also notes that Flash-Control does not identify the coupling buffers as either the first or second buffer or argue that that the buffers are connected to a volatile memory. *Id.* Ultimately, Intel argues that Flash-Control primarily relies on a two-sentence passage in the "Background" of the patent to demonstrate support of a written description, but this disclosure cannot serve as the sole support for a written description. *Id.* (citing ECF No. 60 at 11). Intel notes Dr. Bagherzadeh's admission that these two sentences relate to the static random-access memory preferred embodiment that is not claimed in the asserted patents and that they disclose nothing about the second buffer of the asserted claims. *Id.* at 14–15 (citing Bagherzadeh Dep., 229:7–22, 242:20–243:19, 249:1–12). Intel also notes that the passage does not refer to the first buffer, the second buffer, or the volatile memory at all. *Id.* at 15. Additionally, Intel points out that Dr. Bagherzadeh admitted that a POSITA would be unable to implement writing to the volatile memory at the level below a page based on these two sentences. *Id.* (citing Bagherzadeh Dep., 249:13–24). Intel concludes that the passage might suggest that one might be able to write to memory at the bit or byte level, but the passage is ultimately insufficient as a written description even when combined with the buffers disclosed elsewhere in the specification such that the claims might be obvious. *Id.*

The Court finds Intel's arguments compelling. Intel successfully presented issues with the specification that result in certain limitations lacking written description. In addition, Intel's reply rebuts every point raised by Flash-Control to support the presence of a written description.

More generally, the Court agrees with Intel that Flash-Control's expert improperly relied on the claims for written description support. *See* 35 U.S.C. § 112, ¶ 1. ("The *specification* shall contain a written description of the invention") (emphasis added). Because of the significance of that error, the Court disregards Dr. Bagherzadeh's opinions. Furthermore, the Court agrees with Intel that Flash-Control incorrectly mixed-and-matched citations to different embodiments rather than pointing to a single embodiment that supports all limitations of the asserted claims. *See Novozymes A/S v. DuPont Nutrition Biosciences APS*, 723 F.3d 1336, 1349 (Fed. Cir. 2013). For example, Flash-Control incorrectly attempts combine the embodiment in Figure 9 together with the generic controller in Figure 3. Not only does this incorrectly combine two separate embodiments (to the extent that Figure 3 is an embodiment), Flash-Control does not explain how a POSITA would know to combine an internal component within Figure 3 with the other memories in Figure 9, let alone how to combine them.

In addition, the Court finds that several Flash-Control's arguments are deficient. First, Flash-Control's argument that a POSITA would understand that the specification discloses a second buffer in Figure 3, Figure 6a, or both is misplaced.[1] *See* ECF No. 60 at 6–7 (citing Bagherzadeh Decl. at ¶¶ 37–38). Figure 6a below depicts the functional block diagram of then-current NAND flash chip architecture by Samsung. '880 Patent at 2:58–59.

[1] The Court relies on both its experience with and knowledge of microprocessors and memory systems accumulated over two decades to determine the understanding of a POSITA in the remainder of this section.



A POSITA would not understand that the "data register" and "cache register" in Figure 6a discloses a second buffer and/or volatile memory for at least the following reasons.[2] First, a POSITA would understand that both the data register and cache register are internal to the NAND flash array. But, by contrast, because the first buffer and the volatile memory are separate the nonvolatile memory (*i.e.*, flash memory) from the second buffer, a POSITA would understand that the asserted claims require that the second buffer is *external* to the NAND flash array. Second, a POSITA would understand a "register" holds a single piece of information (*e.g.*, information associated with a single write request) and may be fairly small, *e.g.*, 16- or 32-bits. By contrast, the asserted claims describe that the second buffer holds information corresponding to potentially several write requests, which individually or collectively could be very large. Third, a POSITA

[2] Because the arguments for/against these two components being the second buffer or the volatile memory are the same, the Court will only refer to the second buffer, although the Court's reasoning also applies to the volatile memory as well.

would not understand a "register" to be a generic memory, but rather one that has a more specialized purpose. For example, a condition code register ("CCR") is a group of status flag bits, *e.g.*, overflow, carry, etc. that are generated by various computations. By contrast, the second buffer is not a specialized purpose memory like a CCR, but rather a general purpose memory as it stores information for all write requests. The specification consistently uses labels such as "cache," "buffer," and "latch" to describe more general purpose memories while using "register" to describe more special purpose memory. *Compare* '880 Patent at 2:15-17 ("The preferred embodiment adds new commands to be executed in the Command Register of the NVM (nonvolatile memory)."); 3:64–4:2 ("All these concepts can configure the multiple functions of the device or combination thereof by (1) control/command signals, (2) programmable registers, (3) mode registers, (4) command register, etc.—they can reside in part or in whole in controller, memory, special control, command, interface chip or even CPU.") *with* 1:54–58 ("The 'page' architecture in NAND indeed has 'static latches' that can temporarily store data as a buffer (one page per block), and sometimes have an additional 'write cache buffer for the whole IC.'"); 4:6–9 ("It should be made clear that the 'pages' and 'buffers' mentioned in these pages titled 'NVMS' do not necessarily have to be (1) static latches (6 transistor latches) or (2) traditional SRAM's."); 4:54–57 ("As described in earlier pages, the page latches are available for reading.").

Figure 3 below depicts the "various components of a controller for the nonvolatile memory system (NVMS) of this invention." '880 Patent at 2:52–53.

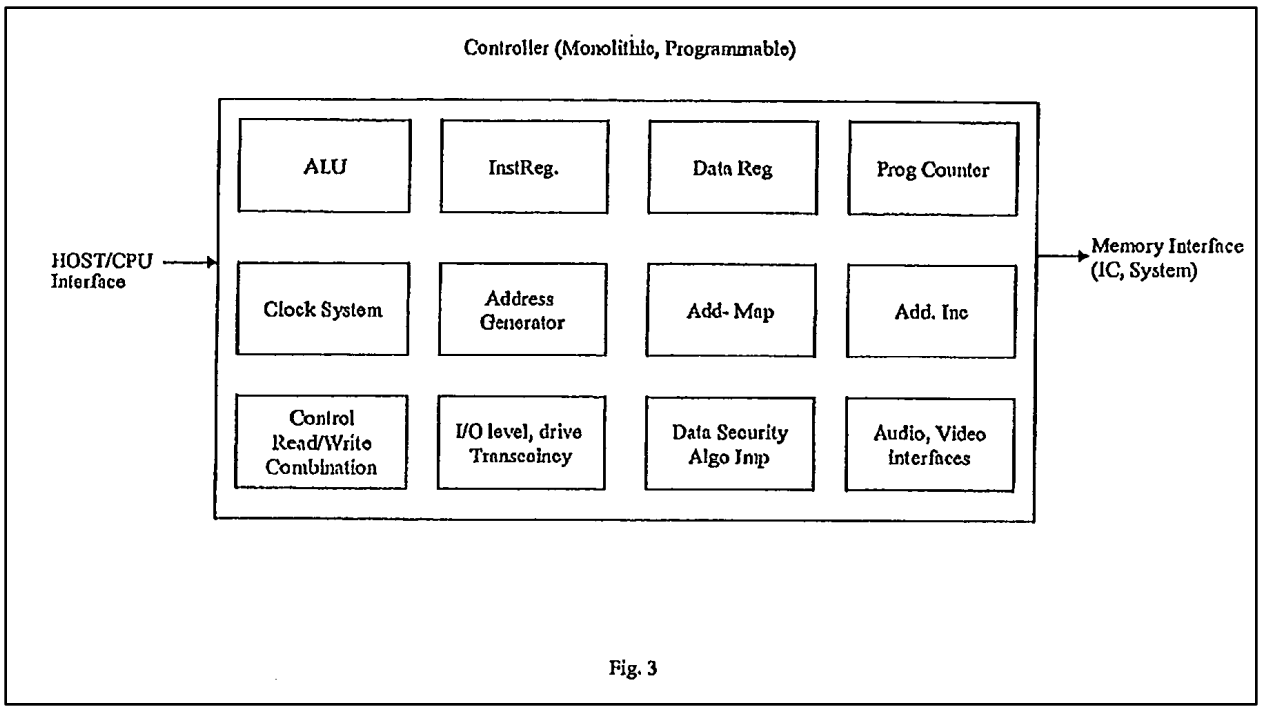


Fig. 3

Figure 3 depicts a controller with several functional components, including an arithmetic logic unit (ALU), instruction register, data register, program counter (Prog. Counter), etc. Given that the controller has interfaces for the host/CPU and the memory, a POSITA would understand that the controller sits between the host/CPU and the memory, and thus is external to both.

A POSITA would also not understand that the "data register" in Figure 3 discloses a second buffer for at least the following reasons. First, a POSITA would understand that the purpose of the "data register" is to provide temporary storage for *data* acted upon by the controller. For example, the controller may add the value in the data register with another value (*e.g.*, from memory). As such, it is not the purpose of the data register to temporarily cache information associated with the write request. If the data register was used in that way, depending on the instruction set of the controller, such usage would block execution of any ALU instruction that performed operations on the data register, thus completely stopping execution of the controller. Second, the width (*i.e.*, number of bits) of a data register in a controller is very small, perhaps as few as 16- or 32-bits. As

such, a POSITA would not understand that a 16-bit or 32-bit data register could be used to store information associated with multiple write requests as described by the asserted claims.[3] Third, even if the width of the data register was sufficient to store information associated with multiple write requests, a POSITA would understand that using a data register in that way would entail too much "overhead" in the form of executing several instructions with read-after-write dependences between them and the associated memory latency. Fourth, for the third reason described with respect to the Figure 6a, a POSITA would not understand that a "data register" in Figure 3 discloses a second buffer.

Second, Flash-Control's reliance on Figure 9 is also misplaced for at least two reasons. First, Figure 9 only discloses three of the four components depicted in the Court's diagram provided above. More specifically, Figure 9 appears to disclose the non-volatile memory and the first buffer. But then, at most, the read/write buffer in Figure 9 discloses the volatile memory only or the second buffer only, but not both. Second, even if the read/write buffer somehow functioned as a combination of the volatile memory and the second buffer, there is no reference or description of the read/write buffer functioning in that manner, let alone any written description of the operation between those two components.

Third, contrary to Flash-Control's assertion, the Court also agrees that purely naming commands is not enough for a written description. *See id.* at 15. The naming of "new commands"

[3] To the extent that Flash-Control contends that a POSITA would understand that the data register is a "register file" (*i.e.*, multiple data registers) the Court disagrees with that argument for at least two reasons. First, Figure 3 plainly depicts the data register as a single data register, as opposed to multiple data registers, *e.g.*, "data registers" or "data register file." Second, a POSITA would understand that controllers are smaller and less powerful versions of a microprocessor. Concomitantly, the former needs, and thus has, fewer data registers than the latter. In light of that understanding, a POSITA would not understand that the "data register" disclosed in Figure 3 is more than one register.

such as "read byte out of page" and "write byte out of page" without illustrations of their functions does not connote possession of claimed invention to a POSITA. *See id.* at 16 (citing '880 Patent at 4:30–36; '537 Patent at 4:31–39). By contrast, these commands are descriptions of the prior art and, by definition, do not disclose the claimed invention. As the invention claims a more efficient implementation of the commands in the context of accessing a non-volatile memory at the granularity of a page, simply reciting the high-level concept will not suffice. Furthermore, even if the Court assumes that the second buffer is present, the Court finds Intel's argument regarding the missing functionality of the second buffer to write on portions smaller than a page persuasive. *See id.*

Ultimately, the Court agrees with Intel's arguments regarding the lack of written of description. With no remaining genuine issue of material fact, the Court grants the Motion for Summary Judgment.

b. Indefiniteness of Claim 1 of '880 Patent

Intel argues that claim 1 of the '880 Patent fails to sufficiently define its scope required under Section 112. ECF No. 48 at 17. Intel asserts that the claim is missing a key claim limitation that would allow a POSITA to understand with reasonable certainty how the data transferred from the volatile memory to the first buffer is updated. *Id.* As such, Intel contends that a POSITA would not be able to distinguish which of the "said one or more changes" are written from the volatile memory to the first buffer. *Id.* at 18. Intel points to Claim 1 of the '537 Patent which discloses "write said one or more updated portions from said volatile memory to said first buffer." *Id.* at 19 (citing '537 Patent at 5:26–30). Intel points out that this language is missing from claim 1 of the '880 Patent which means that all changes, all changes as well as additional information, or a selection of changes could be moved to the first buffer. *Id.* As such, Intel argues that the multiple

possible ways to update the first buffer make it impossible to determine the coverage of the claim. *Id.*

Intel further argues that the lack of an antecedent basis for "said one or more updated portions" adds to the uncertainty of the scope. *Id.* at 20. Intel contends that the claim should be deemed indefinite because the claim had not previously identified the "updated portions." *Id*. Intel points out that the intrinsic evidence is insufficient to fill the gap in the claim since, as stated above, the specification lacks any description of moving or modifying a portion of a page. *Id.* Intel adds that the file history confirms that the claim issued with a missing limitation but contends that the missing limitation cannot be relied upon as part of the intrinsic evidence. *Id.* at 20–21.

Flash-Control argues that a POSITA would have understood that "said one or more updated portions" refers to the said one or more portions of the page associated with the write requests previously written to the volatile memory mentioned in the preceding limitation. ECF No. 60 at 14. Flash-Control contends that Claim 1 of the '880 patent references "changes to one or more portions of a page" which are associated with "write requests" and "updates." *Id.* (citing '880 Patent at 5:2–4, 18–20). Flash-control asserts that Intel's brief acknowledges that "updating" functionally refers to "writing." *Id.* at 16 (citing ECF No. 48 at 18). Flash-Control points out that this association indicates with reasonable certainty to a POSITA that writing changes from the second buffer to the volatile memory results in the first buffer being updated with the changes. *Id.* at 15. Flash-Control also notes that Intel's expert, Dr. Sechen, agreed that a POSITA would have understood that the claim included this option as one of the three options. *Id.* (citing Sechen Decl. at 15:4–10).

Flash-Control also notes that a POSITA would not have understood that the scope covers Intel's proposed alternatives of updating a portion of the page, the entirety of the page, or the page

plus more data. *Id.* Additionally, Flash-Control argues that the claim would not be indefinite even if three different methods of updating existed. *Id.* at 15. Flash-Control contends that a claim encompassing multiple ways of updating a page is not indefinite, ambiguous, or in any way not understandable. *Id.* (citing *In re Gardner*, 427 F.2d 786, 788 (CCPA 1970)). Flash-Control relies on this argument to refute Intel's citation to case law stating that reading language into a claim would result in a claim with impermissible breadth of scope. *Id.* at 17–18. Flash-Control argues that Intel's assertion regarding the lack of antecedent basis for "said one or more updated portions" is also incorrect as an "antecedent basis can be present by implication." *Id.* (citing *Energizer Holdings v. International Trade Com'n*, 435 F.3d 1366, 1371 (Fed. Cir. 2006); '880 Patent at 5:20–21; ECF No. 48 at 20). Flash-Control contends that a POSITA would have readily understood the implicit antecedent as said one or more portions of the page associated with the write request(s) that were previously written to the volatile memory and then changed with data from the second buffer in the preceding limitation. *Id.* Flash-Control argues that the claim clearly indicates that the change results in the first buffer being updated with the changes associated with the write requests. *Id.*

Flash-Control further argues that the alternatives proposed by Intel are inaccurate. Flash-Control contends that the prior step referenced by Intel is incorrect and misconstruing the claim as claim 1 is not a method claim. *Id.* at 17. Flash-Control also notes that Intel implicitly recognizes that "updates," "changes," and "write requests" are associated through its focus on "changes" within the alternatives. *Id.* Flash-Control reiterates that "said one or more updated portions" has an implicit antecedent, so Intel's contention that "updating" could have multiple meanings is inaccurate. *Id.*

In its reply, Intel argues that the claim fails to inform with reasonable certainty a POSITA of the invention's scope due to the claim's omission of language regarding "said one or more updated portions." ECF No. 63 at 16. Intel points out that Flash-Control originally contended that the phrase was a statement of the intended result and not an actual limitation, but now Flash-Control argues that the phrase has meaning as a limitation. *Id.* at 17 (citing ECF No. 60 at 13). Intel also notes that Flash-Control relies solely on its expert's opinion that the phrase would have Flash-Control's proposed meaning to a POSITA. *Id.* However, Intel argues that Dr. Bagherzadeh's opinion fares no better here as he did not even consider the claim in light of the missing claim language. *Id.* (citing Bagherzadeh Dep. at 326:14–20). Intel asserts that Flash-Control argues that a POSITA would have understood the limitation to refer to one or more of the portions of the page associated with the write request(s) that had been previously written to the volatile memory. *Id.* (citing ECF No. 60 at 16). However, Intel argues that Flash-Control does not analyze why its interpretation of "said one or more updated portions" is the interpretation that a POSITA would adopt or why a POSITA would reject the other possible meanings. *Id.*

Furthermore, Intel alleges that Flash-Control and its expert have not adequately addressed the antecedent basis for the "said one or more updated portions" requirement. *Id.* Intel claims that the basis was found in the twenty-nine words that were omitted from the claim and thus is missing from the claim as issued. *Id.* Intel contends that the claim is invalid with the language missing from the claim and cannot be saved by the Court as a matter of law. Intel also argues that Flash-Control attempts to dismiss Intel's cited authority as inapposite but made no effort to distinguish the cases. *Id.* at 18, n. 7

In coming to its conclusion, the Court recognizes that the issued claims can be utilized to prove that the claim is not indefinite. *See Nautilus Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898,

910 (2014). Intel argues that the claim is indefinite because a POSITA would not be able to tell which of the one or more changes are written from the volatile memory to the first buffer. *See* ECF No. 48 at 17. Intel argues that the changes could encompass all changes, all changes as well as additional information stored in the volatile memory, or only some of the changes. *See id.* However, the Court finds some merit in Flash-Control's argument that a POSITA could come to its proposed meaning. *See* ECF No. 60 at 14. While the Court recognizes that the other alternatives are possible, the Court determines that a POSITA would understand that all changes are written from the volatile memory based on the claim.

While Intel contends that the claim is indefinite because "said one or more updated portions" is missing antecedent basis, Flash-Control argues that a POSITA would understand that the antecedent is understood from the preceding limitation. *See* ECF No. 48 at 20; ECF No. 60 at 17. The Court notes Intel's concern regarding the missing language, but the Court also acknowledges Flash-Control's assertion that the antecedent basis can be implicitly found. *See id.* The Court does have some doubts regarding this reasoning, but the Court ultimately finds that this reasoning prevents a showing of clear and convincing evidence of indefiniteness. *See Microsoft Corp. v. i4i Ltd. Partnership*, 564 U.S. 91, 95 (2011).

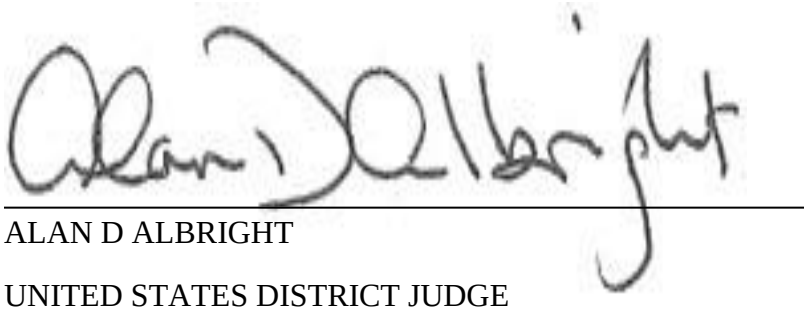
IV. CONCLUSION

As described herein, the Court provides the following constructions:

Term	**Construction**
Whether the Asserted Patents are invalid for lack of written description	Invalid for lack of written description
"said system further adapted to write said one or more changes from said second buffer to said volatile memory, thereby updating said one or more updated portions from said volatile memory to said first buffer, thereby updating said page stored therein to include said one or more changes associated with said one or more write request"	Not indefinite

IT IS THEREFORE ORDERED the Motion for Summary Judgment is **GRANTED** and the case is **DISMISSED** with prejudice. All pending pre-trial motions are **MOOT**.

SIGNED this 21st day of July, 2020.



ALAN D ALBRIGHT

UNITED STATES DISTRICT JUDGE